Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A method for communicating data between a processor and one or more devices over an IDE bus, comprising the steps of:

connecting three or more devices to an IDE bus;

configuring each device as Cable Select; and

providing a device controller that selectively activates at most two of the devices at the same time for data communication over the IDE bus.

2. (currently amended) The method of claim 1, further comprising the steps of, the device controller:

identifying one or two of said three or more devices for data communication with the processor;

selecting a first of the identified devices as a master device;

if more than one device identified, then selecting the second of the identified devices as a slave device; and

activating each selected device, such that a maximum of only two devices among said three or more devices are active at the same time, whereby the activated devices can communicate with the processor over the IDE bus.

3. (Original) The method of claim 2, further comprising the steps of, the device controller receiving identity of said devices for data communication from the processor.

4. (Original) The method of claim 1, wherein the device controller is configured to activate a maximum of two of said three or more devices connected to the IDE bus at a time, and to deactivate the remaining of said three or more devices.

5. (Original) The method of claim 4, wherein the device controller is configured to activate said maximum of two devices by powering the two devices on, and to deactivate said remaining devices by powering said remaining devices off.

6. (Original) The method of claim 1, wherein the device controller is configured to select each of said two devices via a selection signal for each of said two devices.

7. (Original) The method of claim 6, wherein said selection signal comprises the IDE Cable Select line of each device.

8. (Original) The method of claim 1, wherein at least one of the devices on the IDE bus comprises a disk drive.

9. (Original) A method for communicating data between a processor and three or more devices over an IDE bus, comprising the steps of:

(a) deactivating all the devices;

(b) identifying one or two of the devices for data communication with the processor;

(c) selecting a first of the identified devices as a master device;

(d) if more than one device identified, selecting the second of the identified devices as a slave device;

(e) activating each selected device, such that a maximum of only two devices are active at the same time; and

(f) communicating data between the processor and each activated device, over the IDE bus.

10. (Original) The method of claim 9, further comprising the step of:

(g) deactivating all of the devices.

11. (Original) The method of claim 9, further comprising the steps of repeating steps (a) through (f).

12. (Original) The method of claim 9, further comprising the steps of, before step (a), connecting three or more IDE devices to the IDE bus.

13. (Original) The method of claim 9, further comprising the steps of, before step (a), configuring each device as Cable Select.

14. (Original) The method of claim 13, wherein:

step (c) further comprises the steps of selecting the first identified device as a master device via the Cable Select signal for that first device; and

step (d) further comprises the steps of selecting the second identified device as a slave device via the Cable Select signal for that second device.

15. (Original) The method of claim 9, wherein:

in step (a) deactivating each device includes the steps of powering each device off; and

in step (e) activating each selected device includes the steps of powering each selected device on.

16. (Original) The method of claim 9, wherein at least one of the devices on the IDE bus comprises a disk drive.

17. (Currently amended) An Integrated Device Electronics (IDE) interface system for managing data communication between a processor and three or more devices connected to an IDE

bus, the IDE interface system comprising:

a device controller for receiving device control signals to select at least one of said devices for data communication with the processor;

wherein the ~~devices~~ device controller selectively activates at most two of the devices at the same time for data communication with the processor over the IDE bus.

18. (Currently amended) The IDE interface system of claim 17, wherein the device controller is configured to: (a) identify one or two of said three or more devices for data communication with the processor, and receive a signal from the processor to select one or two of the devices identified ~~for data communication~~, (b) in response to the signal, select one of the identified devices as a master device; (c) if more than one device identified, then select the second of the identified devices as a slave device; and (d) activate each selected device, such that a maximum of only two devices among said three or more devices are active at the same time, whereby the activated devices can communicate with the processor over the IDE bus.

19. (Currently amended) The IDE interface system of claim 17, wherein the device controller is configured to activate a maximum of two of said three or more devices connected to the IDE bus at [[a]] the same time, and to deactivate the remaining of said three or more devices.

20. (Original) The IDE interface system of claim 19, wherein the device controller is configured to activate said maximum of two devices by powering the two devices on, and to deactivate said remaining devices by powering said remaining devices off.

21. (Original) The IDE interface system of claim 17, wherein the device controller is configured to select each of said two devices via a selection signal for each of said two devices.

22. (Original) The IDE interface system of claim 21, wherein said selection signal

comprises the IDE cable select line of each device.

23. (Original) The IDE interface system of claim 17, further comprising an interface controller connected to said devices via the IDE bus, wherein the interface controller manages information flow between the processor and said devices over the IDE bus.

24. (Original) The IDE interface system of claim 17, wherein at least one of the devices on the IDE bus comprises a disk drive.

25. (Original) A data storage system comprising:

three or more storage devices connected to an IDE bus for data communication with a processor over the IDE bus; and

a device controller connected to the devices, the device controller for receiving device control signals to select at least one of said devices for data communication with the processor, wherein the device controller selectively activates at most two of the devices at the same time for data communication with the processor over the IDE bus.

26. (currently amended) The data storage system of claim 25, wherein the device controller is configured to: (a) identify one or two of said three or more devices for data communication with the processor, and receive a signal from the processor to select one or two of the devices identified for data communication, (b) in response to the signal, select one of the identified devices as a master device; (c) if more than one device identified, then select the second of the identified devices as a slave device; and (d) activate each selected device, such that a maximum of only two devices are active at the same time, whereby the activated devices can communicate with the processor over the IDE bus.

27. (Currently amended) The data storage system of claim 25, wherein the device

controller is configured to activate a maximum of two of said three or more devices connected to the IDE bus at [[a]] the same time, and to deactivate the remaining of said three or more devices.

28. (Original) The data storage system of claim 27, wherein the device controller is configured to activate said maximum of two devices by powering the two devices on, and to deactivate said remaining devices by powering said remaining devices off.

29. (Original) The data storage system of claim 25, wherein the device controller is configured to select each of said two devices via a selection signal for each of said two devices.

30. (Original) The data storage system of claim 29, wherein said selection signal comprises the IDE cable select line of each device.

31. (Original) The data storage system of claim 25, further comprising an interface controller connected to said devices via the IDE bus, wherein the interface controller manages information flow between the processor and said devices over the IDE bus.

32. (Original) The data storage system of claim 25, wherein at least one of the devices on the IDE bus comprises a disk drive.

33. (New) The data storage system of claim 25 further comprising:

a USB-to-IDE controller connected between the IDE bus and the processor, such that the storage devices are connected to the USB-to-IDE controller via the IDE bus;

wherein the device controller selectively activates the devices for data communication with the processor via the USB controller and the USB-to-IDE controller over the IDE bus.

34. (New) The data storage system o f claim 33 further comprising:

a USB controller connected to the processor, wherein the USB-to-IDE controller is connected between the IDE bus and the USB controller, such that the device controller selectively activates the devices for data communication with the processor via the USB controller and the USB-to-IDE controller over the IDE bus.